

TITLEIMPROVED METHODS AND APPARATUSES FOR RECEIVING AND TRANSMITTING  
SIGNALSFIELD OF THE INVENTION

1 This invention relates generally to transmitters, receivers, and transceivers for transmitting and receiving digital information between two or more digital devices. Certain aspects of the invention relate to solid state receivers, transmitters, and transceiver, including largely, or totally, monolithic devices fabricated on a single semiconductor die.

BACKGROUND OF THE INVENTION

2 In many fields of communication between two or more computers such as those used in military avionics, tanks, howitzer systems and the like wherein digital and analog information must be processed between computers, it has been a common practice to drive the inputs of a transmitter section of one transceiver with digital data which is then appropriately processed in the transmitter and used in turn to drive an output transformer. This output transformer may be connected in one of several available transformer configurations, and the output transformer is in turn connected to a standard bus line and data link and is operative to convert the digital data to an analog voltage of a specified wave shape, waveform timing and power level. These later parameters must be sufficient to properly

transmit the analog data from the transceiver over the bus line and to a similar transceiver located at a remote computer within the particular communication system.

3       For example, in certain military aircraft avionics systems, there might be one such computer in the aircraft cockpit to provide pilot information from another remotely located computer operative for providing various aircraft operational parameters such as speed, direction, fuel levels, temperatures, wind velocities and the like. These two physically separated computers would therefore each be equipped with one or more transceivers which are connected over relatively short data bus links typically on the order of 300 feet or less.

4       In the past, it has been a common practice to use several hybrid connections in the fabrication of a transceiver of the type described above. This practice required that a common insulating substrate such as a ceramic material be used to support and provide electrical interconnections between various components on the substrates such as one or more integrated circuit die, discrete capacitors, thin film resistors, and the like. The requirement for these hybrid circuit interconnections and associated fabrication assembly processes had the disadvantage of providing the additional space required to accommodate the substrate size, and more importantly the disadvantage of increased production costs and decreased device reliability associated with these hybrid fabrication and interconnection processes.

5        Two patents which illustrate prior art transceivers are U.S. Patent 5,153,466 issued on October 6, 1992 to Stein, et al., entitled "All Monolithic Transceiver Operative From A Low Voltage Vcc Dc Supply" (the "Stein Patent"); and U.S. Patent 5,838,722 issued to Michael Consi on November 17, 1998, entitled "Monolithic transceiver including feedback control" (the "Consi Patent"). Both the Stein Patent and the Consi Patent are hereby incorporated herein in their entirety by reference.

SUMMARY OF THE INVENTION

6        An object of one aspect of the present invention is to provide a solid state transmitter or transceiver which avoids undesirable current transients.

7        Another object of one aspect of the present invention is to provide a transmitter or transceiver which can be used with different types of transformers.

8        Yet another object of one aspect of the present invention is to provide a transmitter or transceiver which tends to cause the current flow which it drive in both directions across a transformer to be relatively equal, so as to prevent DC current through the transformer.

9        Still another object of one aspect of the present invention is to provide a transmitter, receiver, or transceiver which can better deal with voltage swings on the transformer to which it is connected.

10 Yet another object of one aspect of the present invention is to provide an operational amplifier, the output of which can more easily be used for different purposes.

11 Still another object of one aspect of the present invention is to provide a transmitter or transceiver which has protection from excessive current flows in its output transistors.

12 The objects set forth above as well as further and other objects and advantages of the present invention are achieved by the embodiments of the invention described below, as well as by other embodiments of the invention not shown.

13 According to one aspect of the invention, a transceiver for driving and receiving a signal through a transformer is provided. The transceiver has an FET power transistor having an output contact for conducting current to a coil of a transformer. The power transistor has a control gate with a parasitic capacitance. The transceiver also has a gate drive circuit which provides a controlled current flow to and from the gate, so as to charge and discharge the gate and its parasitic capacitance, and so as to increase and decrease the output current supplied by the output of the power transistor in a controlled manner. The drive circuit controls the current flow by causing a voltage level that drives the current to compensate for changes in the voltage on the gate so as to make the rate at which the current flows more even during the charging and discharging.

14        In some embodiments of this aspect of the invention there are two of the power transistors, each with an associated output contact. This includes a first power transistor for driving current across a transformer in a first direction during one part of an output signal cycle, and a second power transistor for driving current across the transformer in an opposite direction during another part of the output signal cycle. In such embodiments each of the two power transistors has a corresponding gate drive circuit for charging and discharging its control gate.

15        In some of these two power transistor embodiments the first and second power transistors are each one transistor of a first and second complimentary pair of power transistors, respectively. In such embodiments each complimentary pair includes two power transistors connected in series across a power supply with an associated output contact connected between them.

16        In some of these two power transistor embodiments each gate drive circuit uses a constant current source to charge its associated control gate during at least a majority of the charging of that gate.

17        In some of these two power transistor embodiments the transceiver includes a receiver input circuit, which has a pair of input connections for connection to each side of a transformer coil and for receiving the voltage differential across that coil. Circuitry provides an output measurement signal which varies as a function of the received voltage differential. Such transceivers further include a feedback circuit for stopping the current flow to the control gate of one of the power transistors driving

current across the transformer when the output measurement signal indicates the received voltage differential has reached a desired level.

18        According to another aspect of the invention an output circuit for driving a signal includes an FET power transistor having an output contact and having a control gate with a parasitic capacitance. The output circuit has a gate-drive circuit that provides a controlled current flow to and from the gate to charge and discharge the gate and its parasitic capacitance, so as to increase and decrease, respectively, the output signal supplied by the output of the power transistor at a controlled rate. The drive circuit controls the current flow by causing a voltage level that drives such current to compensate for changes in the voltage on the gate so as to make the rate at which such current flows more even during the charging and discharging. The output circuit also has feedback circuitry that senses the output signal and substantially stop current flow to or from a control gate when it senses that the output signal has reached a desired level.

19        In some embodiments of this aspect of the invention the output circuit is designed for driving an output signal on each of two output contacts so a differently phased version of the output signal is supplied to each such contact. In these embodiments there are at least two power transistors, a first for driving current corresponding to the output signal from its output contact in a first phase and a second power transistor for driving current corresponding to the output signal from its output contact in a second phase. Each of the first and second

power transistors has a corresponding gate drive circuit for charging and discharging its control gate at a controlled rate.

20 In some of these dual phase embodiments, the feedback circuitry senses a voltage difference between the two differently phased outputs and substantially stops current to or from the control gate on one or more of the power transistors when it senses that the voltage difference has reached a desired level.

21 In some of these dual phase embodiments each of the gate drive circuits uses a substantially constant current source to charge its associated control gate during at least a majority of the time spent charging that gate.

22 According to another aspect of the invention a transceiver for driving and receiving a signal through a transformer is provided which includes: a pair of input connections for receiving an input signal from a transformer coil; receiver circuitry for amplifying the input signal and producing an amplified input signal; transmitter circuitry including one or more output transistors for driving an output signal; and pairs of output connections from which the output signal can be connected across the transformer coil, including a first pair for driving a center tapped transformer and a second pair for driving a bridge transformer.

23 In some embodiments of this aspect of the invention, at least a part of the transceiver is constructed as a single monolithic circuit that includes: the input connections; at least

part of the receiver circuitry; at least part of the transmitter circuitry; and the first and second pair of output connections.

24 Some embodiments of this aspect of the invention include a center tapped transformer and the first pair of output connections are connected across that transformer to drive the output signal across it. In such embodiments the pair of input connections are connected across the center tapped transformer to receive the differential voltage across that transformer as the input signal; and the transceiver includes feedback circuitry for using a comparison between the amplified input signal and a desired signal level to control the amplitude of the output signal generated by the transmitter circuitry.

25 In some such embodiments having a center tapped transformer, each of the first pair of output connections has isolation circuitry for electrically isolating it from the transmitter circuitry during different portions of the output signal; and the output connections of the second pair of output connections do not have such isolation circuitry. In some such embodiments the transceiver's circuitry is designed to operate on a single polarity power supply.

26 In some such embodiments including a center tapped transformer, the transceiver is powered by a power supply having a given power supply voltage range; the receiver circuitry includes for each input connections an associated resistor and input operational amplifier. Each input connection is connected through its associated resistor to a virtual ground at one input to its associated input amplifier. The virtual ground at one

input of each input amplifier is maintained through feedback current from the amplifier's output that causes a variable voltage drop through the associated resistor as the voltage on the associated input connection varies. Thus, even if a voltage received at an input connection ranges outside the power supply voltage range, the voltage at the virtual ground input into the associated input amplifier will remain substantially constant, and, thus, will remain within the power supply voltage range.

27        In some such embodiments the receiver circuitry includes circuitry for using the input amplifier feedback currents to generate an amplified input signal which varies as a function of the differential voltage across the transformer to which the input connections are connected. These embodiments including an output control feedback loop for responding to the difference between the amplified input signal and a desired signal level to control the amplitude of the output signal.

28        According to another aspect of the invention a transmitter for driving an output signal through a transformer is provided. This transmitter includes: transmitter circuitry including one or more output transistors for driving the output signal; and pairs of output connections from which the output signal can be connected across the transformer coil, including a first pair for driving a center tapped transformer and a second pair for driving a bridge transformer. Each of the first pair of output connections has isolation circuitry for electrically isolating it from the transmitter circuitry during a different portion of the output signal, whereas the output connections of the second pair of output connections do not have such isolation circuitry.

29        According to another aspect of the invention a transceiver for driving and receiving a signal through a transformer is provided which includes the following: a pair of input connections for receiving an input signal from a transformer coil; receiver circuitry for amplifying that input signal and producing an amplified input signal; transmitter circuitry including one or more output transistors for driving an output signal; pairs of output connections for connecting the output signal across the transformer coil, including a first pair for driving a center tapped transformer and a second pair for driving a bridge transformer; and feedback circuitry for using a comparison between the amplified input signal and a desired signal level to control the amplitude of the output signal. Each output connection of the first pair of output connections has isolation circuitry for electrically isolating it from the transmitter circuitry during a different portion of the output signal; and the output connections of the second pair of output connections do not have such isolation circuitry.

30        Some embodiments of this aspect of the invention include a center tapped transformer, and the first pair of output connections are connected across that transformer to drive the output signal across it; and the input connections are connected across the center tapped transformer to receive the differential voltage across it as the input signal.

31        According to another aspect of the invention a transmitter for driving an output signal through a transformer having a center tapped winding is provided. The transmitter includes: a

pair of input connections for connection across the center tapped winding so as to receive the differential voltage across the winding; transmitter circuitry including one or more output transistors for driving an output signal; a pair of output connections from which the output signal can be connected across the center tapped winding of the transformer, where each output connection of the pair has isolation circuitry for electrically isolating it from the transmitter circuitry during a different portion of the output signal; and feedback circuitry for using a comparison between the received differential voltage and a desired signal level to control the amplitude of the output signal.

32 In some embodiments of this aspect of the invention such a transmitter is included in a transceiver for both driving and receiving signals through a center tapped transformer. The transceiver includes receiver circuitry connected to the pair of input connections for producing an amplified input signal which varies as a function of the received differential voltage.

33 In some embodiments of this aspect of the invention the one or more output transistors are FET transistors each having an output contact and a control gate with a parasitic capacitance. The transmitter circuitry includes a gate drive circuit that provides a controlled current flow to and from the gate of each output transistor to charge and discharge that gate and its parasitic capacitance, so as to increase and decrease the output signal supplied by the output contact of the output transistor. The drive circuit controls the current flow by causing the voltage level that drives such current to compensate for changes

in the voltage on the gate so as to make the rate at which such current flows more even during the charging and discharging. The feedback circuitry substantially stops the flow of current to or from the control gate as a function of the comparison between the received differential voltage and the desired signal level.

34 According to another aspect of the invention a receiver for receiving a signal generated across a winding of a transformer is provided. The receiver includes: a pair of input connections for receiving a differential voltage input from opposite sides of the transformer winding; and a separate operational amplifier associated with each of the two input connections. Each such op amp includes two inputs, a first of which is connected to a reference voltage, and at least one output connected to the second of the amplifier's inputs to form an operational amplifier feedback loop which holds that second input at a virtual ground. The receiver further includes a separate resistor associated with each of the two input connections, connected between the input connection and the virtual ground at the second input of the input connection's associated amplifier, so that current in the operational amplifier feedback loop can flow through the resistor to the associated input connection to help hold the amplifier's virtual ground at its associated reference voltage. As a result, even if a voltage received at an input connection ranges outside the receiver's power supply voltage range, the voltage at the virtual ground input into the associated input amplifier will remain substantially constant, and, thus, within that power supply voltage range.

35 In some embodiments of this aspect of the invention the receiver is part of a transceiver which includes: transmitter circuitry including one or more output transistors for driving an output signal; and a pair of output connections for driving a center tapped transformer, with each connection of the pair having isolation circuitry for electrically isolating it from the transmitter circuitry during different portions of the output signal; circuitry for producing an output measurement signal as a function of the feedback currents in the two input amplifiers, which signal varies as a function of the differential voltage supplied between the input connections; and feedback circuitry for using a comparison between the output measurement signal and a desired signal level to control the amplitude of the output signal.

36 Some such transceivers are designed for a power supply voltage between ground and a given power voltage, and the transceiver is designed so that when the output connections and input connections are connected to opposite ends of a center tapped transformer and the transmitter circuitry drives the output signal, the voltages received at the input connections range on the opposite side of ground from the given power voltage.

37 According to some embodiments of the receiver of this aspect of the invention the input amplifier connected to a first of the input connections produces a first feedback current which is a function of the voltage of the first input connection. The input amplifier connected to a second of the input connections produces a second feedback current which is a function of the first

feedback current minus a feedback current generated by the input amplifier which is proportional to the voltage of the second input connection. Circuitry is provided for producing an amplified input signal as a function of the second feedback signal.

38 According to some embodiments of this aspect of the invention each input amplifier has two outputs, with circuitry causing substantially equal current to flow in each output even if the load on those outputs differ. One of the outputs is connected to provide the feedback current necessary to maintain the virtual ground at the amplifier's second input, and the other output producing an equal current used for another purpose.

39 According to another aspect of the invention an operational amplifier is provided which has two inputs; two outputs; and circuitry for causing substantially equal current to flow in each of the two outputs even if the loads on them vary.

40 In some embodiments of this aspect of the invention the circuitry for causing substantially equal current to flow in each of the two outputs includes similar circuitry to drive each such output, including similar transistors connected to similar control voltages.

41 In some embodiments of this aspect of the invention the circuitry for causing substantially equal current to flow in each of the two outputs includes a separate complementary pair of output transistors driving each such output, with each output transistor of each such pair having a corresponding cascode

transistor to cause its current to be less affected by variations in the voltage of each such complementary pair's output.

42 According to another aspect of the invention a transmitter for driving an output signal through a transformer is provided which includes: transmitter circuitry including one or more output transistors for driving the output signal; a pair of output connections from which the output signal can be connected across the transformer coil; circuitry for producing a measurement of current flow across one or more of the output transistors; and circuitry for substantially turning off current flow in the one or more output transistors for at least a given time period when the current measurement exceeds a given level.

43

In some embodiments of this aspect of the invention the transmitter is powered by a power supply having two voltage rails, and there are at least two complimentary pairs of the power transistors, each having two output transistors connected in series between the voltage rails with a node between them to which the pair's associated output connection is connected. The transmitter circuitry includes circuitry for driving the two complimentary pairs, so that one pair can drive current in a first direction across the transformer during one part of an output signal cycle, and the other pair can drive current in an opposite direction across the transformer during another part of the output signal cycle. Each output transistor in each complimentary pair has associated circuitry for producing the measurement of current flow across it. The circuitry for substantially turning off current flow in the one or more output transistors substantially turns off current flow in all of the

output transistors in response to a measurement that current flow in any one of the output transistors exceeds a given level.

44        In some embodiments of this aspect of the invention at least a part of the transmitter is constructed as a single monolithic circuit. This monolithic circuit includes: the output transistors; at least part of the circuitry for measuring; and at least part the circuitry for substantially turning off are all on one semiconductor chip. In one such embodiment the monolithic circuit further includes: external connections for providing transistor drive signals to one or more external power transistors which can be used for driving an output signal across a transformer; an external current overflow connection for receiving an indication of a current overflow in one or more of the external power transistors; and circuitry for responding to such an indication of an external overflow by substantially turning off the transistor drive signals.

45        Some embodiments of this aspect of the invention are transceivers which include such a transmitter. Such transceivers further include: a pair of input connections for receiving an input signal from a transformer coil; and receiver circuitry for amplifying that input signal and producing an amplified input signal.

46        In some embodiments of this aspect of the invention the transmitter generates the output signal in response to a digital sequence of one or more successive output bits received from other circuitry; and the circuitry for substantially turning off current includes latching circuitry for keeping the current

turned off, once it has been turned off, until the next end of a sequence of successive output bits is received from the other circuitry. The latching circuitry is reset after the next end of a sequence of successive output bits, so that a later sequence of successive output bits received from the other circuitry can cause the transmitter to generate another output signal.

47        In some embodiments of this aspect of the invention the circuitry for producing a measurement includes a current sensing resistor in series with the current flowing through one or more output transistors.

48        The invention also includes methods of operating transmitters, receivers, and/or transceivers which are similar to the methods of operation of the apparatus described above.

#### BRIEF DESCRIPTION OF THE DRAWINGS

49        FIG. 1 is a block diagram showing the overall design of a transceiver according to one embodiment of the invention;

50        FIG. 2 is a detail of the receiver input section of the transceiver shown in FIG. 1;

51        FIG. 3 is a schematic diagram of an operational amplifier with two outputs, corresponding to amplifiers 200 and 202 shown in FIG. 2;

52        FIG. 4 is a detail of the receiver output section of the transceiver of FIG. 1;

53        FIG. 5 is a detail of an output drive circuit, such as the circuits 434 and 436 shown in FIG. 4;

54 FIG. 6 illustrates the transmitter section of the transceiver of FIG. 1 in greater detail, with the portion of FIG. 7 encircled in dotted lines being shown in a highly simplified manner in that figure, and being shown with greater accuracy in FIGS. 7 and 8;

55 FIG. 7 is a schematic diagram of the transmitter section's output transistors and their drive circuitry;

56 FIG. 8 is a schematic diagram of the transmitter section's transmitter enable circuits and overcurrent detection circuits;

57 FIG. 9 illustrates how the circuitry of FIG. 1 can be connected to drive a 5 volt center-tapped transformer;

58 FIG. 10 illustrates how the circuitry of FIG. 1 can be connected to drive a 15 volt center-tapped transformer;

59 FIG. 11 is a schematic diagram of one possible external drive circuit for use with a 15 volt center-tapped transformer of the type shown in FIG. 10; and

60 FIG. 12 is a schematic diagram of the common bias circuits which are used by the other sections of the circuitry shown in FIG. 1.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

61 FIG. 1 shows an embodiment of the invention which is a transceiver IC designed to connect electronic equipment to a MIL-STD-1553 serial data bus. Other embodiments of the invention can be used with other types of data buses.

62 The transceiver of FIG. 1 consists of a receiver input section 6, a receiver output section 8, a transmitter section 10,

and some common bias circuits 12 which supply bias currents and bias voltages 40-68 to the other sections, all of which are located on a monolithic integrated circuit. The transmitter and the receiver input are connected to the data bus 2 through a transformer 4. To meet a variety of different applications, the monolithic transceiver of FIG. 1 can be used with different types of transformers, as will be explained below.

RECEIVER INPUT SECTION:

63        Signals from the data bus 2 pass through the transformer 4 to RXIN\_H 18 and RXIN\_L 20 at the receiver input section 6. Details of the receiver input section are shown in FIG. 2.

64        The signal from RXIN\_H 18 passes through weighting resistor 206 to a virtual ground 210 at the inverting input of an operational amplifier 200. The signal from RXIN\_L 20 passes through an equal weighting resistor 208 to a virtual ground 212 at the inverting input of another operational amplifier 202. Both virtual grounds are held very close to the bandgap reference voltage BGREF 68 (about +2.4 volts, from the bias circuits) by feedback around the op amps.

65        Although it is not shown in FIG. 2, there are three different pairs of receiver input connections 18 and 20, each having a differently weighted corresponding pair of resistors 206 and 208. Each of these different pairs is designed to connect the receiver input to a different transformer.

66        200 and 202 are operational amplifiers each having two outputs with substantially identical output currents. A schematic diagram of this amplifier is shown in FIG. 3. The two outputs 300 and 310 are created by connecting the gates of identical transistors 302-308 and 312-318 in parallel to the same control inputs. Aside from the multiple outputs, the amplifier design is familiar to one skilled in the art: a differential pair 320 driving a common-source stage 308 and 318, with cascode current sources 302-304, 312-314, etc.. The cascode transistors 304-306 and 314-316 cause the current flow through each of the op amp's outputs 300 and 310 be less affected by variations in voltage at those outputs. This tends to cause the currents which pass through these two outputs to be substantially identical, even if the loads on them vary considerably.

67        The first output of 200 must supply all of the current that passes through the weighting resistor 206 from RXIN\_H 18. The second output of 200 delivers an identical current to the virtual ground 212 at the input of 202, where it subtracts from the current through the other weighting resistor 208 from RXIN\_L 20, thus 200 acts as a current mirror. The first output of 202 must supply a current, through a feedback resistor 214, that is equal to the difference between the two input currents, thus 200 and 202 combine to act as a differential amplifier.

68        When the transmitter is operating, the transmitter output voltages TXOUT\_H 14 and TXOUT\_L 16 are seen at RXIN\_H 18 and RXIN\_L 20. This output voltage will vary depending on the type of transformer being used. As stated above, a separate pair of input connections 18 and 20, each with different resistors 206

and 208, is provided for each different transformer used with the transceiver. For any transformer, the two weighting resistors 206 and 208 are scaled so that the difference current at the virtual ground 212 is typically  $+-0.5\text{mA}$  when the transmitter output voltage is correct for the transformer being used. This scaling of the weighting resistors also compensates for the effect of the transformer on signals received from the data bus, so that the receiver sees signals of consistent amplitude regardless of what transformer is being used.

69 Connecting the input connections RXIN\_H and RXIN\_L to the virtual grounds 210 and 212 created by the op amps 200 and 202 has the benefit of causing the voltages which reach the transistors of the receiver circuitry in FIG. 2 to remain within the voltage range of the unipolar power supply supplied to the transceiver of FIG. 1, even if voltages induced in the transformer connected to that transceiver go outside that range. This is particularly important if the transceiver is used with a center tapped transformer. This is because, when the transceiver first drives one half of the center tapped winding of such a transformer with the power supply voltage in one direction and then drives the other half of that winding with the same power supply voltage in another direction, the half of the transformer winding which is not being currently driven will have a voltage of the opposite polarity to that driving the other half induced in it. This will cause voltages received on one of the two input connections RXIN\_H and RXIN\_L to be below ground, and, thus, outside the voltage range of the transceiver's power supply during each half of each output signal cycle. The use of the virtual grounds 210 and 212 isolates all of the circuitry FIG. 2

except for portions of the resistors 206 and 208 from these out of range voltages.

70        The voltage at the first output of 202, labeled FEEDBACK 22, is sent to the transmitter section, where it is used to regulate the amplitude of transmitter output voltages. When the output voltage is correct for the transformer being used, FEEDBACK 22 is typically +/-1 volt.

71        The second output of 202 passes an identical current through resistor 216, which is at the input to a filter. The voltage drop across resistor 216 is much larger than the FEEDBACK signal 22, so a pair of clamping transistors 228 divert current away from 216 to limit the signal amplitude. The slew rate at this point is limited by a capacitor 218 in parallel with resistor 216.

72        A third operational amplifier 204 is used to implement an active filter which reduces the amount of noise in the filtered signal 24. This filter is the current-input equivalent of a standard voltage-input filter familiar to those skilled in the art. It is a three-pole low pass filter with a corner frequency near 3 MHz. The filtering is performed by a feedback network of resistors and capacitors 216-226. Another feedback network of two resistors 230-232 gives the filter a gain of two at low frequencies.

## RECEIVER OUTPUT SECTION:

73        The filtered signal 24 from the receiver input section goes to the receiver output section 8. Details of the receiver output section are shown in FIG. 4.

74        As is shown in FIG. 4, the filter output signal 24 is compared to the bandgap reference voltage BGREF 68 by two comparators 402 and 404 with complementary outputs. A current of about 100uA from the bias circuits 12, shown in FIGS. 1 and 12, passes through resistor 406 to set the connection VTHP 66 to the bias circuits to about 0.4 volts above the filter output voltage 24; another 100uA current passes through resistor 408 to set the connection VTHN 62 to the bias circuits to about 0.4 volts below the filter output voltage 24. These currents set the input threshold voltages for positive and negative signals. If the filter output signal is below the negative threshold, comparator 402 will set BELOW\_L 410 high; otherwise NOT\_BELOW 412 will be high. If the signal is above the positive threshold, comparator 404 will set ABOVE\_H 414 high; otherwise NOT\_ABOVE 416 will be high.

75        If the receiver enable input RXENA\_H 30, which, as is shown in FIG. 1, is a signal from outside the transceiver which can be used to control its operation, is high, the signals on BELOW\_L 410 and ABOVE\_H 414 will be passed to the receiver outputs RXOUT\_L 28 and RXOUT\_H 26 respectively. BELOW\_L high will drive RX\_LOW 422 low, which will drive RXOUT\_L high. ABOVE\_H high will drive RX\_HIGH 424 low, which will drive RXOUT\_H high.

76        If the filter output 24 is between the high and low threshold voltages, NOT\_BELOW 412 and NOT\_ABOVE 416 will both be high, and the outputs will be controlled by the RX\_IDLE input 32, which, as is indicated in FIG. 1, is a signal from outside the transceiver which can be used to control its operation. RX\_IDLE high will drive BETWEEN 426 low, which will drive both RXOUT\_H and RXOUT\_L high. RX\_IDLE will also control the outputs if RXENA\_H 30 is low; then RX\_IDLE high will drive DISABLE 428 low, which will drive both RXOUT\_H and RXOUT\_L high.

77        Each of the receiver outputs 26 and 28 is driven by an output drive circuit 436 or 434, respectively. Each of these outputs is protected from electrostatic discharges (ESD) by two very large transistors 502 and 504, shown in FIG. 5, which divert surges of electric current into either the positive power supply or into ground. These ESD clamping transistors 502 and 504 also function as output drive transistors on the RXOUT\_L and RXOUT\_H lines, respectively.

78        Details of the output drive circuits 434 and 436 are shown in FIG. 5.

79        Transistors 502 and 504 are the large transistors protecting the output. Transistors 506 and 508 are much smaller transistors, connected to the larger transistors to form current mirrors. Resistors 510 and 512 provide some additional protection against ESD currents.

80        Each output drive circuit has a signal input 430 or 432 and an enable input 438. If the signal input is low and the enable

input is high, current will flow through transistor 506, making output transistor 502 conduct, which pulls the output, labeled 26 or 28 in FIG. 4, high. If the signal input and the enable input are both high, current will flow through transistor 508, making output transistor 504 conduct, which pulls the output 26 or 28 low. The maximum high or low output current can be set by adjusting the dimensions of transistor 506 or 508. If the enable input is low, all the transistors will be off, but transistor 502 will conduct if an ESD surge drives the output voltage above the positive supply voltage, and transistor 504 will conduct if an ESD surge drives the output voltage below ground.

#### TRANSMITTER SECTION:

FIG. 6 shows a greatly simplified version of the transmitter section. The portion of this figure which is shown encircled in dotted lines omits many features of the actual transmitter, to more simply explain the basic operation of the circuit. The four output drive transistors 700-706 are connected in a configuration that is sometimes referred to as an H-bridge, and are controlled by some input logic gates.

82 The transmitter input logic determines whether the transmitter has a valid command to drive its output high or low. Two NOR gates 600 and 602 monitor the transmitter inputs TXIN\_H 36 and TXIN\_L 38 and the transmitter enable input TXENA\_L 34. If TXIN\_H is high, TXIN\_L is low, and TXENA\_L is low, then there is a valid command to drive the transformer high, so NOR gate 600

will drive TX\_HIGH 604 high. TX\_HIGH will turn on transistors 700 and 706, driving TXOUT\_H 14 high and TXOUT\_L 16 low.

83        If TXIN\_H is low, TXIN\_L is high, and TXENA\_L is low, then there is a valid command to drive the transformer low, so NOR gate 602 will drive TX\_LOW 606 high. TX\_LOW will turn on transistors 702 and 704, driving TXOUT\_H 14 low and TXOUT\_L 16 high.

84        For any other combination of input signals, no valid command is recognized. TX\_HIGH 604 and TX\_LOW 606 will both remain low. All four output transistors will remain off, and signals may be received from other transmitters on the data bus.

85        As is indicated above, the portion of FIG. 6 which is shown encircled in dotted lines 603 is shown in a highly simplified, somewhat inaccurate, form to provide a quick overview of the basic function of the transmitter circuitry. FIGS. 7 and 8 provide a more detailed and accurate diagram of the circuitry corresponding to that shown within those dotted lines in FIG. 6. FIG. 7 is a detailed schematic diagram of the transmitter output transistors and their drive circuits. FIG. 8 shows the transmitter enable circuits and the overcurrent detection circuits.

86        As shown in FIG. 7, the gates of the four main output drive transistors 700-706 are driven from the I\_TX\_RT current source 50 in the bias circuits section shown in FIGS. 1 and 12. This current is steered by a differential pair 730 and a series of current mirrors 732-740 to drive the gates of all four drive

transistors. The drive transistors are very large, so they have large gate-to-source and gate-to-drain parasitic capacitances which are charged and discharged slowly by the gate drive current. The  $I_{TX\_RT}$  current source is a constant current source, and it causes the current supplied to the gate of each output transistor by its corresponding current mirror to be substantially constant during a substantial portion of the time during which that current flows onto or off of each output transistor gate. Thus, the  $I_{TX\_RT}$  current source causes the rise and fall of the transmitter output voltages and currents to occur at a relatively constant rate.

87 Each current mirror includes a turn-on transistor for supplying current to, and a turn-off transistor for drawing current from, the gate of its associated output transistor. The transistors of the current mirrors are weighted so the turn-off transistors pass current faster than the turn-on transistors. This causes one output transistor in each complementary output pair to be substantially shut off before the other transistor in that pair is substantially turned on, causing the output drive transistors 700-706 to exhibit a desirable "break-before-make" behavior which limits the current surges that flow while the drive transistors are switching.

88 If  $TX\_HIGH$  604 in FIG. 8 is high, the  $I_{TX\_H}$  current source 54 in the bias circuits section will sink about 100uA of current from the ERROR summing node 746 to ground. As is shown near the middle of FIG. 7, this current flows through resistor 748 to the FEEDBACK signal 22. The voltage drop across resistor 748 pulls ERROR 746 about one volt below BGREF 68, so the current from

$I_{TX\_RT}$  50, reflected through current mirror 732, is steered by the differential pair 730 into current mirrors 734 and 740. Mirror 734 turns transistor 702 off and transistor 700 on, pulling the OP output 750 high. Mirror 740 turns transistor 704 off and transistor 706 on, pulling output ON 754 low. Because N-channel transistors conduct more readily than P-channel transistors, a diode-connected transistor 744 is used to limit the gate voltage of transistor 706.

89        If  $TX\_LOW$  606 in FIG. 8 is high, the  $I_{TX\_L}$  current source 58 in the bias circuits section will source about 100uA of current to the ERROR summing node 746 from the positive power supply through a current mirror 802. As shown near the middle of FIG. 7, this current flows through resistor 748 to the FEEDBACK signal 22. The voltage drop across resistor 748 pulls ERROR 746 about one volt above  $BGREF$  68, so the current from  $I_{TX\_RT}$  50, reflected through current mirror 732, is steered by the differential pair 730 into current mirrors 736 and 738. Mirror 738 turns transistor 700 off and transistor 702 on, pulling the OP output 750 low. Mirror 736 turns transistor 706 off and transistor 704 on, pulling output ON 754 high. Because N-channel transistors conduct more readily than P-channel transistors, a diode-connected transistor 742 is used to limit the gate voltage of transistor 702.

90        In either case, it takes about 200nS for the gate drive current to charge and discharge the gate capacitances of the four output drive transistors 700-706. For a majority of this time the current flow to or from each of those transistor's gates is substantially constant. The circuitry which drives this gate

current keeps it substantially constant over such a period by varying the voltage it uses to drive such current so as to compensate for factors which might otherwise cause such current to vary, such as changes in gate voltage as the power transistors' gates are charged or discharged.

91        After about 200nS, the FEEDBACK signal 22 changes to reduce the difference between the ERROR 746 voltage and BGREF 68. As this difference between ERROR and BGREF gets small the current from I\_TX\_RT 50 will begin to divide between the current mirrors 734-740, which decreases the previously substantially constant currents which were charging or discharging the gates of the output transistors. When the transmitter output voltage approaches its final value, the difference between ERROR 746 and BGREF 68 is reduced ultimately to nearly zero, and the current from I\_TX\_RT 50 is divided equally among the gate drive current mirrors 734-740, which substantially stops the current flow to the gates of the output transistors .

92        It is important to note that the FEEDBACK signal 22 from the receiver input section depends on the differential voltage across the entire primary winding of the transformer, not on the voltage from one side of a center-tapped transformer to ground. Some prior art, including the Consi Patent previously mentioned, contains feedback to control the output voltage from one side of a center-tapped transformer to ground. But it is possible for a center tapped transformer to have primary windings that are not exactly equal, so that the two sides of the transformer need to be driven with slightly different voltages in order to avoid an unbalanced current flow through the transformer. The

differential feedback used in the present invention can automatically compensate for this effect, thereby avoiding any DC current flow which might tend to distort the transmitted signals.

93       As is indicated in FIG. 7, when the transmitter is turned off, the transmitter enable signals TXE\_H 804 and TXE\_L 806 block the gate drive current at transistor 728, and the four transistors 720-726 force the gate-to-source voltage of each output drive transistor 700-706 to zero, thereby turning off all four output drive transistors.

94       When a valid TX\_HIGH 604 or TX\_LOW 606 command is received from the transmitter input logic, TXDLY\_L 808 in FIG. 8 is pulled low, driving TXE\_H 804 high and TXE\_L 806 low to enable the four output drive transistors 700-706. DELAY 810 is also pulled low, discharging capacitor 812. As long as the intervals between valid TX\_HIGH 604 and TX\_LOW 606 commands are not long enough to permit capacitor 812 to charge up to the bandgap reference voltage BGREF 68 through transistor 814, which acts as a 25uA current source, then TXDLY\_L 808 remains low and the transmitter remains turned on. When no more TX\_HIGH 604 or TX\_LOW 606 commands are received, capacitor 812 charges up to BGREF 68 in about 400nS, then TXDLY\_L 808 rises and the transmitter turns off. This 400nS delay before turning off the transmitter allows the transmitter output to return to zero volts under control of the feedback loop.

95       If any one of the four output drive transistors 700-706 exceeds about 1 Ampere of current, it will trip the overcurrent shutdown circuits. Each drive transistor is connected to a 0.2

ohm current sense resistor 710-716, shown in FIG. 7. The voltages SENSE1 to SENSE4 from each sense resistor 710-716 are compared to 0.2 volt reference voltages 820-826 by four dedicated comparator circuits 830-836 shown in FIG. 8. If comparator 832 or 836 detects excessive current in transistor 702 or 706, the comparator will pull OVC\_N 838 low, which in turn pulls OVC\_H 840 high. If comparator 830 or 834 detects excessive current in transistor 700 or 704, the comparator will pull OVC\_H 840 high directly. If the external overcurrent input OVC\_EXT 844 is pulled low, it will also pull OVC\_H 840 high; this external input permits an external drive circuit to trip the overcurrent shutdown circuits.

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The overcurrent shutdown circuits include latching circuitry which will keep the output drive transistors turned off during a sequence of successive output bits. Once OVC\_H 840 is pulled high by one of the comparators 830-836, OVC\_H will shut off TXE\_H 804 and TXE\_L 806, thereby turning off the four output drive transistors 700-706. OVC\_H high will also force OVC\_L 842 low. The OVC\_H and OVC\_L signals form a pair of cross-coupled NAND gates which latch the overcurrent signal. The latch is cleared when TXDLY\_H 816 is pulled low by the transmitter enable circuit, after no TX\_HIGH 604 or TX\_LOW 606 commands have been received for about 400nS. Thus if an overcurrent shutdown occurs during a sequence of successive output bits received from other circuitry, the transmitter will remain shut down until the end of the sequence of successive output bits. The latching circuitry is reset after the end of the sequence of successive output bits so that a later sequence of successive output bits received from other circuitry will cause the transmitter to generate another

output signal. This has the advantage of protecting the output drive transistors from excessive currents, while permitting the transmitter to resume normal operation after the overcurrent problem has ended.

97 The transmitter output drive circuits can drive three different types of transformers, to meet a variety of different applications. In all cases, the secondary winding of the transformer is connected to the data bus.

98 As shown in FIG. 1, the transmitter uses the 5 volt power supply to drive a transformer 4 with a single primary winding; this is referred to as the 5 volt bridge connection. The 5 volt bridge connection uses the four output drive transistors 700-706 shown in FIG. 7 connected as an H-bridge. The transformer is connected to the pair of output connections marked OP 750 and ON 754 in FIG. 7.

99 In FIG. 9, the transmitter uses the 5 volt power supply to drive a transformer 4 with a center-tapped primary winding (such as, for example, a Technitrol Q1553-45 or equivalent), where the center tap is connected to ground; this is referred to as the 5 volt center-tapped connection. The transformer is connected to the pair of output connections marked CTP 752 and CTN 756 in FIG. 7. The 5 volt center-tapped connection uses two additional transistors 708 and 718 with their gates grounded, as shown in FIG. 7. These additional transistors and their connection to ground, electrically isolate each of the output connections 752 and 756 from the rest of the transmitter circuitry when the voltage on such a connection goes below ground, so the CTP and

CTN outputs can swing below ground in response to voltages induced in the currently un-driven half of the center tapped winding without having an adverse effect on the operation of the transmitter circuitry.

100        In FIG. 10, the transmitter is shown using an external circuit 100 operating on a +15 volt or -15 volt supply to drive a different transformer 4 with a center-tapped primary winding (which could be, for example, a Technitrol Q1553-2 or equivalent), where the center tap is also connected to ground; this is referred to as the 15 volt center-tapped connection. In the 15 volt center-tapped connection, the external drive circuit is connected to the pair of output connections CTP 752 and CTN 756, which are shown in both FIGS. 7 and 10.

101        One possible embodiment of the external drive circuit 100 is shown in FIG. 11. Two transistors 1102 and 1104 shift the CTP and CTN output voltages down to the -15 volt VEE supply, where two other transistors 1106 and 1108 drive the transformer drive outputs TXOUT\_H 14 and TXOUT\_L 16. The external circuit contains an overcurrent shutdown circuit similar to the internal overcurrent shutdown circuits contained in the monolithic circuit. If the current through resistor 1110 exceeds about 0.3 ampere, the external overcurrent signal OVC\_EXT 844 is pulled low to set the internal overcurrent latching circuitry in the monolithic circuit, thereby turning off the CTP and CTN outputs and shutting down the external drive circuit.

## BIAS CIRCUITS SECTION:

102 FIG. 12 is a schematic diagram of the common bias circuits which are used by the other sections. These bias circuits include a bandgap voltage reference, a startup circuit, a bias current regulator, and several adjustable current sources.

103 The bandgap voltage reference circuit is familiar to one skilled in the art. Two transistors 1200 and 1202 have equal bias currents and unequal areas. The base-to-emitter voltage of each transistor has a negative temperature coefficient. The difference between their base-to-emitter voltages has a positive temperature coefficient. This difference voltage is amplified by differential pair 1204 and common source transistor 1206, and added to the base-to-emitter voltage to drive the bandgap reference voltage output BGREF 68. Feedback to the transistors is attenuated by two 2:1 voltage dividers 1208 and 1210, so that BGREF is approximately 2.4 volts.

104 The startup circuit operates only when the positive power supply voltage AVDD first turns on. As the power supply voltage rises above 1 volt, transistor 1212 pulls the STARTUP signal 1214 high. STARTUP turns transistor 1216 on, which keeps common source transistor 1206 turned off to allow the BGREF 68 voltage to rise, while transistor 1218 turns on to start bias currents flowing through several P-channel cascode current sources controlled by two bias voltages PMIR 1220 and PBIAS 1222. One of these bias currents flows through two N-channel transistors to create two additional bias voltages NMIR 1224 and NBIAS 1226. As all of these bias currents approach normal values, transistor

1228 pulls STARTUP 1214 low, turning transistors 1216 and 1220 off.

105        At this point, a bias current regulator circuit takes control of the bias currents. Differential pair 1232 drives transistor 1230, forcing the voltage at the top of resistor 1234 to equal BGREF 68. With 2.4 volts across resistors 1234 and 1236, the current through transistor 1230 into the bias circuits is approximately 100uA.

106        The bias currents can be adjusted if desired, although such adjustments are not necessary for proper operation of the transceiver. The voltage at the TRIM\_IREF input 42 is normally 1.2 volts. If TRIM\_IREF is adjusted above or below 1.2 volts, a current will flow through resistor 1238 into either resistor 1234 or resistor 1236, so that the current through transistor 1230 can be trimmed to exactly 100uA. To facilitate such trimming, an additional current source IREF 40 is provided where the actual bias current can be measured while making this adjustment.

107        Six adjustable current sources are connected to bias voltages NMIR 1224 and NBIAS 1226. These current sources can be trimmed above or below 100uA by adjusting the voltage at their respective trim inputs in a manner similar to the TRIM\_IREF input previously discussed. Each current source controls a different parameter of the transceiver, and each of these parameters can be adjusted by trimming its respective current source. VTHP 66 and VTHN 62 control the threshold voltages for low and high input signals in the receiver as shown in FIG. 4; VTHP also uses a current mirror 1240 to reverse its direction.

I\_TX\_H 54 and I\_TX\_L 58 control the high and low signal output voltages from the transmitter; these are the currents that flow into the ERROR signal 746 in FIG. 8, which is compared to the FEEDBACK signal 22 in FIG. 7. I\_TX\_RT 50 controls the rise time of the output voltages from the transmitter; this is the current that charges and discharges the gates of the output drive transistors 700-706 in FIG. 7. I\_TX\_IS 46 controls the bias current sources shown in FIG. 8, and sets the current limiting threshold of the overcurrent detection circuits in the transmitter by controlling the four 0.2 volt reference voltages 820-826 used by the four dedicated comparator circuits 830-836 as shown in FIG. 8.

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It should be understood that the foregoing description and drawings are given merely to explain and illustrate, and that the invention is not limited thereto except insofar as the interpretation of the appended claims are so limited. Those skilled in the art who have the disclosure before them will be able to make modifications and variations therein without departing from the scope of the invention.

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In particular, it should be noted that this application explains the present invention in more detail than is common in many patent applications, by showing actual circuit schematics for one embodiment of the invention rather than just functional block diagrams having blocks corresponding to recited claim elements. The inventor hopes he will not be punished for providing the public with such a detailed teaching by having the scope of his claims limited to details shown in such schematics which would not be included in such functional block diagrams.

Punishing a more detailed teaching of an invention with a more limited interpretation of the claims would be contrary to one of the primary purposes of the patent system, which is to reward inventors for teaching their inventions to the public. In this application, it is intended that each claim be interpreted just as broadly as if this specification had included a separate block diagram having blocks and connections corresponding to each of the claim's recited elements and relationships between elements. Since such block diagrams would add no information to the application, and since their number would greatly impede any reading of this application, an effort has been made to make this application more readable by excluding such diagrams.

110

Considerable thought has been put into the wording of the following claims so that they will provide an accurate description of the scope of what the inventor considers to be his invention, and it is hoped that the meaning of the claims will be interpreted from their own wording rather than from the particulars of the one or more embodiments of the invention described in the specification. For example, where a dependent claim includes limitations not contained in a parent claim, the parent claim is meant to be read as not including that limitation, unless common sense would require a contrary interpretation among those skilled in the relevant technical art.

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In addition, those skilled in the electronic arts will understand that many of the circuits and circuit functions described in the claims, can be designed or performed in many different ways. Thus, the claims are not meant to be limited to the exact circuitry shown in the drawings. To cite just one of

many possible examples, this application includes claims which recite "feedback circuitry for using a comparison between said received differential voltage and a desired signal level to control the amplitude of said output signal." Feedback circuits are well known in the electronic arts, and people skilled in those arts know what the above quoted language means and would be able to quickly design many very different circuits capable of achieving such feedback control which would come within the intent of such claim language. Thus, the claims should not be limited to the precise wiring of the corresponding circuitry shown in the figures.

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In the embodiments of the invention discussed above, almost all of the various aspects of the invention are shown occurring together in one transceiver system. It should be understood that in other embodiments of the invention different subsets of one or more individually claimed aspects of the invention can occur in a given system. Here are just a few of many possible examples of this point: not all embodiments of some aspects of the invention need to be transceivers, some can be transmitters and some can be receivers; not all embodiments of aspects of the invention need have current overflow shut off circuitry; not all receiver circuitry needs to use operational amplifiers with feedback loops providing a virtual ground for receiving input from a transformer; and not all receiver circuitry which does use such op amps needs to use op amps which each have two outputs with substantially equal current.

113

It should be understood that some aspects of the invention are intended to cover a receiver, transmitter, or transceiver

designed for use with a transformer, even when it is not currently connected to a transformer. Not all aspects of the invention are limited to use or intended use with transformers. Embodiments of some aspects of the invention could be designed to communicate through other media, such as RF transmissions, coaxial cables, twisted pair, fiber optics, just to name a few. In fact, some aspects of the invention relating to op amps with two outputs are not even limited to use on transmitters, receivers, or transceivers.

114        Some aspects of the invention recite the use of FET output or power transistors, but others do not and embodiments of such other aspects of the invention can use other types of transistors, such as bipolar transistors.

115        The op amps used in some aspects of the invention have two outputs each, but in other aspects of the inventions op amps having only one output can be used. For example, those skilled in the art will understand how each two-output op amp shown in FIG. 2 could be replaced by two single-output op amps.

116        According to some aspects of the invention, the outputs of the input op amps corresponding to amplifiers 200 and 202 of FIG. 2 could be combined in different ways to produce a signal which measures the differential voltage generated across the transceiver's transformer. For example, the outputs of each of the two input op amps could be supplied to two inputs of a differential amplifier to produce such a signal. Furthermore, in some embodiments, the input amplifier circuits could be other

than operational amplifiers, and amplification could be of either voltage and/or current.

117        In the embodiment of the invention shown, virtually all of the components necessary for the transceiver, except its transformer, are provided in one monolithic integrated circuit. In embodiments of many aspects of the invention greatly different degrees of integration could be used.

118        As those skilled in the electronic arts will appreciate, in most cases electronic signals can be measured, or responded to, either based on their voltage or their current. Unless claims relating to a particular aspect of this invention make clear that one of the other of these two characteristics is to be used for such measuring or responding, it should be understood that either could be used.

119        In general, a statement in the claims that an element is connected to another element is not meant to require that they be directly connected. In many embodiments intermediary components could exist between such connected elements. For example, the recitation in some claims of a complementary pair of output transistors connected in series across a power supply is not meant to exclude the possibility of other components in series with them between those power rails.

120        The aspects of the invention that relate solely to operational amplifiers having two similar current outputs are not intended to be limited to use with a transmitter, receiver, or transceiver.

121        In many aspects of the invention relating to receiving an input signal generated across a transformer it is not necessary that the input signal be connected to virtual ground nodes, as is shown FIG. 2. Such inputs can be supplied to amplification circuitry using other previously known techniques for making such connection.

122        In the embodiment of the invention described above, a current overflow causes the transceiver's power transistors to be turned off and to remain off as long as a continuous sequence of bits is being supplied to the transceiver for transmission. In other embodiments of this aspect of the invention the current overflow circuitry could turn the power transistors off for different periods of time, such as, for example, a fixed period of time, or until the transceiver receives an external signal.

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